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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,617	08/25/2003	Robert Servilio	18090	2864

26794 7590 10/17/2006

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EXAMINER	
BAYARD, EMMANUEL	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 10/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

3F

Office Action Summary	Application No.	Applicant(s)	
	10/647,617	SERVILIO ET AL.	
	Examiner	Art Unit	
	Emmanuel Bayard	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Wessel et al U.S. patent No 6,275,685.

As per claim 1, Wessel et al teaches a method for dynamically correcting an aspect of an electromagnetic wave being processed, said method comprising the steps of: processing two or more aspects of said electromagnetic wave along two or more separate signal paths (see figs.4-5 elements 42, 602 and col.7, lines 15-45); comparing (see fig.5 element 630 and col.7, lines 35-40]) an expected value for at least one of said aspects of said electromagnetic wave along at least one of said signal paths with an actual value for said aspect of said electromagnetic wave along said at least one signal path to generate a correction signal (see fig.5 element 82 or 84 and col.7, lines 45-67) and applying said correction signal to at least one other aspect of said electromagnetic wave (see figs. 4, 6 element 92 and 94 and col.6, lines 50-67).

As per claim 2, Wessel et al teaches, wherein said two or more aspects of said electromagnetic wave comprise amplitude and phase information (see figs.4-6 elements 42, 602 and col.7, lines 15-45) for said electromagnetic wave.

As per claim 3, Wessel et al teaches wherein said aspect of said

electromagnetic wave that is compared is phase information (see fig.5 element 630]) for said electromagnetic wave.

As per claim 4, Wessel et al teaches, wherein said step of applying said correction signal to said other aspect of said electromagnetic wave is accomplished by compensating for an analog delay (see col.6, lines 59-62 and col.8, lines 35-41).

As per claim 5, As per claim 3, Wessel et al teaches wherein said actual value is digitized into a digital signal using a quantizer (see fig.6 element 704 and col.9, lines 63-65 and col.10, lines 35-37).

As per claims 6, 11 and 19, Wessel et al teaches wherein said step of comparing said expected value to said actual value is accomplished using a digital phase-locked loop (see figs 4-7.).

As per claims 7, 12 and 20, Wessel et al teaches, wherein said step of applying said correction signal to said other aspect of said electromagnetic wave is accomplished using RAM and buffer are the same as the claimed (a bank of pipeline registers) (see fig.6 elements 710, 728, 740, 758 and col.8, lines 5-45).

As per claim 8, Wessel et al teaches wherein said step of applying said correction signal to said other aspect of said electromagnetic wave is accomplished by compensating for a digital delay (see fig.6 elements 716, 746 and col.8, lines 50-67 and col.9, lines 47-60).

As per claims 9 and 13, Wessel et al teaches wherein said step of applying said correction signal to said other aspect of said electromagnetic wave is accomplished by determining a digital delay (see fig.6 element 716, 746) between at least two of said

aspects of said electromagnetic wave using a difference in clock periods (see col.8, lines 35-67)) between at least two of said aspect signals (see fig.5 element 445 and page 3 [0029]).

As per claims 10, 15 and 23, Wessel et al teaches method for dynamically correcting a signal being processed, said method comprising the steps of: processing an amplitude aspect and a phase aspect of said signal along an amplitude and a phase paths, respectively (see figs.4-5 elements 42, 602 and col.7, lines 15-45); quantizing said phase aspect of said signal to generate an actual phase value (see fig.6 element 704 and col.9, lines 63-65 and col.10, lines 35-37); comparing said actual phase value with an expected phase value to determine any delay in an analog portion of said phase path in relation to said amplitude path (see fig.5 element 630 and col.7, lines 35-40]); generating a correction signal based upon said comparison (see fig.5 element 82 or 84 and col.7, lines 45-67); and using said correction signal to adjust said amplitude aspect of said signal (see figs. 4, 6 element 92 and 94 and col.6, lines 50-67).

As per claim 14, Wessel et al teaches wherein said adjustment of said amplitude aspect of said signal is accomplished using at least one pipeline register (see fig.6 elements 710, 728, 740, 758 and col.8, lines 5-45).

As per claim 16, Wessel et al teaches wherein said aspects of said signal comprise amplitude and phase information (see figs.4-5 elements 42, 602 and col.7, lines 15-45.

As per claim 17, Wessel et al teaches wherein said aspect of said signal that is compared is phase information (see fig.5 elements 630 and col.7, lines 15-45.

As per claim 18, Wessel et al teaches wherein said comparison circuit comprises a quantizer for generating said digital value of said one aspect (see fig.6 element 704 and col.9, lines 63-65 and col.10, lines 35-37).

As per claim 21, Wessel et al teaches wherein said comparison circuit further comprises a processor for determining any delay in a digital portion of said one path relative to said separate path using a difference in clock periods between said aspects of said signal along said paths, generating another correction signal, and using said another correction signal to adjust said other aspect of said signal.

As per claims 23 and 25, Wessel et al teaches, wherein said processor comprises RAM and buffer are the same as the claimed (at least one pipeline register using) (see fig.6 elements 710, 728, 740, 758 and col.8, lines 5-45).

As per claim 24, Wessel et al teaches further comprising a processor for determining any delay in a digital portion (see fig.6 element 716, 746) of said one path relative to said separate path using a difference in clock periods along said paths, generating another correction signal, and using said another correction signal to adjust said separate signal path (see fig.5 element 445 and page 3 [0029]).

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Booth et al U.S. Patent No 6,512,417 teaches linear amplifier.

Bengtsson et al U.S. Pub No 2002/0071497 A1

Yamakoshi U.S. Patent No 6,381,292 B1 teaches a phase synchronizing.

Hebron et al U.S. patent No 6,539,068 B2 teaches a receiver.

Masheff et al U.S. Patent No 4,696,017 teaches a quadrature signal.

Gailus et al U.S. patent No 6,449,465 B1 teaches a method and apparatus for linear amplification.

Rosnell et al U.S. patent No 6,993,087 B2 teaches a switching mode power.

Horsfall et al U.S. patent No 6,160,444 teaches a demodulation of FM carrier.

O'Flaherty et al U.S. patent No 6,703,897 B2 teaches a methods of optimizing power.

Eisenberg et al U.S. patent No RE37,407 E teaches a polar envelope correction.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272 3016. The examiner can normally be reached on Monday-Friday (7:Am-4: 30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571 272 2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Emmanuel Bayard
Primary Examiner
Art Unit 2611

10/11/06

EMMANUEL BAYARD
PRIMARY EXAMINER